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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/596,987	07/03/2006	Qingjiang Ma		4082

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EXAMINER	
MALEK, LEILA	
ART UNIT	PAPER NUMBER
2611	

MAIL DATE	DELIVERY MODE
04/14/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/596,987	MA ET AL.	
	Examiner	Art Unit	
	LEILA MALEK	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7,21,22,26 and 27* is/are rejected.

7)☒ Claim(s) *8-20,23-25 and 28-30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 July 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Applicant's claim for the benefit of a prior-filed application under 35 U.S.C. 119(e) or under 35 U.S.C. 120, 121, or 365(c) is acknowledged.

Claim Objections

2. Claims 21-30 are objected to because of the following informalities: as to claims 21-26 numerical references to the drawings (e.g. (100) or (102)) should be removed from the claims. Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-7, 21, 22, and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Leydier et al. (hereafter, referred as Leydier) (US 2004/0148539).

As to claim 1, Leydier discloses a process, comprising the steps of: generating a reference signal (see paragraph 0134, oscillator signal 926 or any other outputs of HSO 900 (see Fig. 10) can been interpreted as reference signal); generating a value (e.g. M 21) equal to a number of cycles of the reference signal in a time duration covering a predetermined number of bit periods (e.g. 4 bits or 8 bits) in a packet in the data stream (see paragraphs 0111 and 0134); generating a clock signal synchronized with the data stream (see paragraph 0135, CLK1X 803 and Fig. 18) by calculating a

number of cycles of the reference signal in a bit period (see paragraph 0134 last two lines) of the data stream from the value and the predetermined number (see also paragraphs 0069, 0079, 0095, 0098, 0103, 0111). Leydier is silent in disclosing that value M 21 is a digital value. However, it would have been obvious to one of ordinary skill in the art at the time of invention to use a digital value at least for the reasons that digital values are easier to generate and at the same time they are more reliable.

As to claim 2, Leydier discloses that the step of generating a reference signal including generating an oscillation signal using an oscillator (see paragraph 0134). Although Leydier does not discloses that the oscillator is a resistor-capacitor oscillator, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Leydier and use a resistor-capacitor oscillator to reduce the cost of the system (since R-C oscillators are less expensive).

As to claim 3, Leydier discloses that the step of generating a value including generating the value equal to the number of cycles of the reference signal in the time duration covering eight bit periods in the packet in the data stream (see paragraph 0135).

As to claim 4, Leydier further discloses that the step of generating a value including generating the value equal to the number of cycles of the reference signal in the time duration from a beginning of second bit (b2) to a beginning of tenth bit (b9) in the packet in the data stream (see paragraph 0135).

As to claim 5, Leydier further discloses that the step of generating a value including the step of identifying the packet in the data stream as a token packet (see

paragraph 0111, lines 2-3 and Figs. 7 and 8) according to a universal serial bus (USB) protocol (see paragraph 0077).

As to claim 6, Leydier further discloses that the step of identifying the packet as a token packet including the step of analyzing first ten bits of the packet (see paragraphs 0080, 0088, and 0103).

As to claim 7, Leydier does not expressly disclose that analyzing the bits of the packet includes analyzing a voltage level. However, in digital communications it would have been clearly recognizable to one of ordinary skill in the art at the time of invention to use voltage level analysis to detect the bits (as evidence for instance see Yellin et al. US 7,240,265) to make the bit detection faster and less complicated.

As to claim 21, Leydier discloses a system comprising: a data input bus (see paragraphs 0005 and 0011); a reference signal generator configured to generate a fixed frequency signal (see Fig. 3, block 395A and Fig. 18, block 395A/900); a digital data analyzer (see Fig. 3, block 395B and Fig. 18, block 395B) coupled to the data input bus (see Fig. 3) and to the reference signal generator (395A), the data analyzer being configured to generate a value (e.g. M 21) equal to a number of cycles of the fixed frequency signal of the reference signal generator in a time duration covering a predetermined number of bit periods (e.g. 4 bits or 8 bits) in a packet in a data stream at the data input bus (see paragraphs 0111 and 0134-0135); and a digital synchronized clock signal generator (see Fig. 3, block 395D and Fig. 18, block 395D) coupled to said data input bus, to the reference signal generator (395A), and to the data analyzer (395B), the digital synchronized clock signal generator being configured

to generate a clock signal (CLK1X 803) synchronized to the data stream in response to the value of the said data analyzer (see paragraph 0134 last two lines). Leydier is silent in disclosing that value M 21 is a digital value. However, it would have been obvious to one of ordinary skill in the art at the time of invention to use digital value at least for the reasons that digital values are easier to generate and at the same time they are more reliable.

As to claim 22, Leydier further discloses that the synchronized clock signal generator (395D) including a counter (see Fig. 14, block 30 and paragraph 0094) configured to count at a rate equal to a frequency of the fixed frequency (i.e. the number of cycles) signal of said reference signal generator.

As to claim 26, Leydier discloses a device comprising: a data processing element (see Fig. 3, block 396 or in general USB device 390) coupled to the host (see Fig. 4, block 300); and a digital synchronization unit (see Fig. 3, block 395) including: an oscillator (see block 395A, HSO High Speed Oscillator)); a data analyzer (see Figs. 3 and 18, block 395B) coupled to the data processing element and to the oscillator, the data analyzer being configured to generate a control signal (e.g. M 21) having a value equal to a number of cycles of a fixed frequency signal of said oscillator (see paragraph 0134, oscillator signal 926 or any other outputs of HSO 900 (see Fig. 10) can been interpreted as fixed frequency signal) in a time duration covering a predetermined number of bit periods (e.g. 4 bits or 8 bits) in a packet in the data stream at said data processing element; and a digital synchronized clock signal generator (see Figs. 3 and 18, block 395D) coupled to the data processing element, to

the oscillator, and to the data analyzer, the digital synchronized clock signal generator being configured to generate a clock signal (CLK1X 803) synchronized to the data stream in response to the control signal (see paragraphs 0069, 0079, 0095, 0098, 0103, 0111, 0134, 0135). Leydier is silent in disclosing that value M 21 is a digital value. However, it would have been obvious to one of ordinary skill in the art at the time of invention to use a digital value at least for the reasons that digital values are easier to generate and at the same time they are more reliable.

4. Claim 27 is rejected under 35 U.S.C. 103(a) as being unpatentable over Leydier, in view of Hansen et al. (hereafter, referred as Hansen) (US 2002/0057682).

As to claim 27, Leydier discloses that the host device can be a personal computer or lap top connected to USB device (see paragraph 0020). However, Leydier does not expressly disclose that the data processing element (USB device) is configured to move a cursor on a screen of a host computer coupled and make commands to the host computer. Hansen, in the same field of endeavor, discloses a system and method for a Universal Serial Bus (USB) device. Hansen further discloses that the USB device (interpreted as data processing element) may include a USB mouse (configured to move a cursor on a screen of a host computer) or a keyboard. Therefore, it would have been obvious to one of ordinary skill in the art at the time of invention to modify Leydier as suggested by Hansen, to allow the user to perform various system-dependent operations.

Allowable Subject Matter

5. Claims 8-20, 23-25, and 28-30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to LEILA MALEK whose telephone number is (571)272-8731. The examiner can normally be reached on 9AM-5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on 571-272-3021. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Leila Malek

Examiner
Art Unit 2611

/L. M./
/Leila Malek/
Examiner, Art Unit 2611

/David C. Payne/
Supervisory Patent Examiner, Art Unit 2611